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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,535	01/27/2004	Cyrus Afghahi	51707/JEJ/B600	1035

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EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 08/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,535	AFGHAHI ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/27/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search Report*.

DETAILED ACTION

1. Claims 1-21 are pending.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: MEMORY DEVICE HAVING SIMULTANEOUS READ/WRITE AND REFRESH OEPRATIONS WITH COINCIDENT PHASES

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 8-10, 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leigh (U.S. Patent No. 5,007,022) in view of Irrinki et al. (U.S. Patent No. 5,808,932).

Regarding claim 1, Leigh discloses, in FIGS. 2 and 3a-3i, a memory circuit comprising:

a plurality of memory cells, organized into columns and rows, that are accessed during memory access cycles, which include refresh cycles and read/write cycles, wherein the memory cells are substantially continuously refreshed using the refresh cycles;

a plurality of sense amplifiers (58, see FIG. 2), wherein each said sense amplifier is coupled to a corresponding one of the columns (22, see FIG. 2) of the memory cells,

and is used to read data stored in the memory cells of the corresponding column during read phases of the memory access cycles;

wherein the read phases of the refresh cycles substantially coincide with the write phases of the read/write cycles, and the write phases of the refresh cycles substantially coincide with the read phases of the read/write cycles (see FIGS. 3a-3i)

(See column 5, line 11 to column 8, line 25).

However, Leigh does not disclose that the write amplifier is used to write data to the memory cells during write phases of the memory access cycles.

Irrinki discloses, in FIG. 5, a memory array having read amplifiers (214-1 to 214-m) used during read phases of the memory access cycles; write amplifiers (512-1 to 512-m) used during write phases of the memory access cycles.

Since Leigh and Irrinki are both from the same field of endeavor, the purpose disclosed by Irrinki would have been recognized in the pertinent art of Leigh.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include write amplifiers of Irrinki in the memory circuit of Leigh for the purpose of amplifying write data inputted externally.

Regarding claims 2-3, Leigh discloses an inherent read/write address generator for generating read and write addresses (Program Address, see FIG. 4); a refresh address generator for generating refresh addresses used to refresh the memory cells (84, see FIG. 4).

Regarding claims 8-10, they encompass the same scope of invention as to that of claims 1-3, except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Regarding claims 15-17, Leigh further discloses, besides limitations in claim 1-3, the memory device is a system on chip (see column 1, lines 13-25), which inherently includes data processing circuitry and I/O port because those are essential memory components.

5. Claims 2-7, 9-14, 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leigh in view of Irrinki et al. further in view of Tanaka (U.S. Patent No. 6,134,169).

Leigh in view of Irrinki disclose, as applied in prior rejection of claims 1-3, all claim subject matter. Leigh further discloses a not-shown circuit for detecting coincidence between read, write, and refresh addresses but not in detail (see column 7, line 62 to column 8, line 3).

Tanaka discloses, in FIG. 3:

Regarding claim 2, a read/write address generator (11).

Regarding claim 3, a refresh address generator (17).

Regarding claim 4, collision avoidance mechanism (18), which prevents an attempt to perform both refresh and read/write operations concurrently on identical said memory cells;

Regarding claim 5, wherein the collision avoidance mechanism compares the refresh addresses with the read/write addresses (via 18) to determine whether the attempt is made to perform both the refresh and read/write operations concurrently in the identical said memory cells;

Regarding claim 6, wherein at least one of the refresh addresses is updated to prevent the attempt to perform both the refresh and read/write operations concurrently on the identical said memory cells.

Regarding claim 7, wherein the at least one the refresh addresses is updated by being changed by at least one.

(See column 3, lines 17-61).

Since Leigh, Irrinki, and Tanaka are all from the same field of endeavor, the purpose disclosed by Tanaka would have been recognized in the pertinent art of Leigh.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include the circuit of Tanaka, FIG. 3, in the memory circuit of Leigh because it is essential for the performance of the memory circuit in Leigh.

Regarding claims 9-14, they encompass the same scope of invention as to that of claims 2-7, except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Regarding claims 16-21, they are rejected under U.S.C. 103(a) since they recite the same limitations as in claim 2-7.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VTN
August 5, 2004

VanThu Nguyen
Primary Examiner
Art Unit 2824